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ENGINEERING PROJECTS.

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1. Overview.

The following are engineering projects which must be completed in the next 12 months. These projects are distributed between WC and BSW engineering groups.

Amiga Projects:

- 68020 Co-processor board for A2000.
- 1024x800 High-Res Mono Adapter and Monitor for Amiga.
- High-Res (640x400 non-interlaced) chipset.
- AT Emulator for A2000.
- Scan Doubler for Amiga.
- 8MB RAM Board for A2000.
- V1.3 Software Release.
- Page (Laser) Printer and Scanner controller.
- A2000 Hard Disk Controller cost reduction.
- A500 Hard Disk Drive Subsystem.
- Mitsumi Genlock for A2000.
- Turbo Upgrade for XT Emulator for A2000.
- UNIX Operating System.
- Paging MMU and Cache chipset.
- A3000, 68020 based Amiga (on motherboard).
- Super B52 (A500 Case, 68020 CPU).
- NYIT Genlock and Framegrabber for A2000.
- A500 Genlock.

PC Projects.

- PC1.
- PC10-CR (XT).
- PC40-CR (AT).
- PC80 (386 CPU, in current PC40 case).
- Baby 386. (PC60?, 386 CPU in PC10-CR/PC40-CR case).

Consumer Product Line Projects.

- 1541-CR.
- 1764 and C64E compatibility resolution.
- 1200 BPS Modem, move to in-house manufacturing.

OEM Projects.

- Source new dual scan Amiga monitors (Color and Mono).
- Source Page Printer Engine (Laser, LCS, etc.)
- Source low cost page scanner.

2. Amiga Project Descriptions.

Below is a short description of each Amiga project.

2.1. 68020 Co-processor board for A2000.

This the board currently being worked on by Bob Welland. It has a 68020 CPU running at approximately 15Mhz, 2MB of 32-bit wide memory, Motorola MMU and Floating point co-processor. However we are also planning to have available a "dummy MMU" chip which plugs into the MMU socket for a pure AmigaDOS version of this board. This could save around $75 over the Unix version. Rough Schedule is:

- Working samples August 28.
- 15 Fully Functional (producable) units by November Comdex. Preliminary release of UNIX available on this board for Comdex.
- Production Startup around end December 1987.
- Costing to be determined within next two weeks.

2.2. 1024x800 High-Res Mono Adapter and monitor.

This is the Hedley Davis project. Current plan is to source high resolution monochrome monitor which supplies additional 5V power to also drive the high-resolution adapter board. The high-res adapter board will then be housed in the tilt and swivel base of this high-res monitor. Note that this approach means it can be used for any Amiga product (A500 and A2000). To meet reasonable cost target, a gate array is required which is now being defined. Note that this gate array is also being used as the test vehicle for internal (MOS) gate array manufacturing. The gate array design tools and rules are compatible with the Toshiba gate array system.

This product also requires substantial software development. Rough schedule is:

- 15 Fully Functional Prototypes by November Comdex.
- Production Startup around early February 1988.
- Final Costing to be determined by end of September.

2.3. 640x400 Chipset.

Second Rev samples of High-Res Fat Agnes will be available by August 31. Very high probability that these will be producable parts. High-res Denise needs more work. Current rev also has some identified problems, however as you know it requires a small tower board to function in the high-res modes. Samples of second rev of High-Res Denise will be available by September 15. However we are trying to incorporate this "tower" board circuitry into the chip. This will result in a pin-compatible (with old Denise) chip which will allow all A500 and B2000 systems to be upgraded without any PCB changes. Rough Schedule is:

- 2nd Rev High-Res Fat Agnes, samples September 15. Production quantities could be available by October 31.
- 2nd Rev High-Res Denise ("tower" board version), samples September 15.
- Pin-Compatible High-Res Denise samples (no tower board required) October 20 (in time for Comdex). If no additional rev required, production quantities could be available by December 15.

2.4. AT Emulator for A2000.

This is a BSW project. My feeling on rough schedule is:

- Start new PCB layout in BSW on Aug 20. Assume three weeks for layout.
- Release BOM for purchasing of all key components (e.g. Faraday chipset, WD Floppy Controller Chip, etc).
- Receive first sample PCBs (mainboard is 4-layer), September 15. Debug and test 10 days.
- If no changes required to PCB artwork, release artwork to production on September 25.

- FCC Scan and filing by no later than October 9.
- As this is a 4-layer board, at least 4 weeks leadtime will probably be required in Germany for production PCBs (at a premium). Hence start production on October 26.
- Receive first production units by November 6, for European shipments. This is optimistic!
- Assuming 7 week FCC approval cycle, earliest FCC approval will be obtained around November 27. This will be limiting factor for USA ship date.
- Cost not yet determined.

2.5. Scan Doubler for Amiga.

The definition and need for this product is still not clear. The reason for this is that the new 640x400 non-interlaced (mono) mode may in fact be satisfactory for solving the productivity issue. However if a 640x400 color (non-interlaced) is still required, a full frame store double scanner may have some value. The major problem with this project is however lack of resources as it competes for the same resources used for the 1024x800 high-res adapter, which we currently feel is a higher priority. Another problem here is that to achieve a reasonable cost a different gate array (than that used for the 1024x800) will probably be required.

2.6. 8MB RAM Expansion board for A2000.

This product is basically ready for production, should it be required. Due to current cost of 1MB DRAMs, the cost of this board is currently around $900. Need more marketing input.

2.7. V1.3 Software Release.

This is a new release of both the kickstart ROM and Workbench software. Main features are:

- Booting from any controller which has a special "boot" ROM, e.g. Hard Disk Controller.
- Major performance improvements in the areas of: file system, text operations and printers.
- Various bugs fixed. Utility improvements.
- Release planned for October 1987.

2.8. Page Printer and Scanner Controller.

This board is both a RAM expansion board as well as a controller for handling direct output to a page (laser) printer engine and input from a page scanner. This board will use 1MBit DRAMs and will be configured with 1MByte of DRAM with sockets for another 1MB. If we can get the cost for the laser engine and page scanner circuitry down to a reasonable amount, this board could be sold as a RAM Expansion board with a "bonus" laser printer and scanner interface. This has some interesting marketing potential. To get the cost down, a gate array will be required. First rev of this board (without gate array) is due September 15.

There are some major software developments required to make this board into a final product, e.g. Epson and HP LaserJet emulation, scaleable font support (Postscript??), etc.

- Target Production Startup is late February 1988.

2.9. A2000 Hard Disk Controller cost reduction.

A custom chip is under development which will result in a major cost reduction of the A2000 Hard Disk Controller. This chip will allow either SCSI Hard Disk Drives or so-called "XT" interface hard disk drives to be used. As the latter are also being used in newer generation PCs, the cost of these "XT" drives may drop faster than SCSI drives. New software drivers required. No cost impact for supporting both types. Rough Schedule:

- Chip definition and logic design completed September 30.
- First Samples of chip November 15.
- New Hard Disk Controller PCB Prototypes, November 15.
- Production startup, February 15, 1988.

- Cost to be determined.

2.10. A500 Hard Disk Controller Subsystem.

This is an external Hard Disk for the A500. Tooling qoutes are being obtained now. A current hardware design exists. We need to determine whether or not to put current hardware design into production or to wait for the new custom chip being developed for the A2000 cost reduction. Using this chip will significantly reduce the cost (at least $15). Need to discuss options and schedule. If new chip is to be used, production startup schedule is approximately the same as A2000 cost reduced hard disk controller.

2.11. Mitsumi A2000 Genlock.

Will finalise schedule with CJL next week. Preliminary schedule is:

- "Final" samples in WC by September 28.
- Functional and FCC Testing complete by October 9.
- Production startup (assuming Mitsumi can start in 60 days), December 15.

2.12. Turbo Upgrade for A2000 XT Emulator.

This project must be started in BSW asap. It is fairly simple and involves using the new Faraday 2010A chip and implementing the "turbo" modes (7.16 and 9.54Mhz clock speeds). We should be able to changeover to this new design by the end of the year.

2.13. UNIX Operating System.

An experimental version of Unix and window manager is now running on an Amiga. However there are some major decsions which have to be taken very soon. The major issue is the Unix System V versus Berkeley Unix (or Mach) controversy. The former is probably the adopted "standard" for Europe whilst the latter is the "standard" in the higher end workstation market (and U.S. university market). As the highest percentage of our sales are now in Europe, it may be wise to go for System V at this stage, even though this will not neccesarily be very acceptable to some U.S. engineers! This decision has major marketing impacts

Supporting both standards will probably not be possible with our limited resources. Final schedules have not yet been determined.

2.14. Paging MMU and Cache chipset.

This is a very important part of the UNIX puzzle as it will allow us to have a high-performance yet low cost paging MMU system. This could save us around $50-65 when compared to using the Motorola paging MMU for the 68020. Current schedule is:

- First samples, November 13.
- Second Rev samples, January 15. This assumes we have some form of working system prototype board to plug these chips into by November 13!

2.15. A3000, 68020 based Amiga (on motherboard).

The A3000 is intended to become the "high-end" Amiga workstation. There are obviously questions as to the exact market to be addressed and how easy or difficult it is for us to market this type of system. However we are going ahead with the architectural design and prototyping of this machine. The general direction and configuration being pursued for this system is:

- 68020 CPU Running at least at a clock rate of 15Mhz.
- Commodore MMU and Cache chips.
- Highres Fat Agnes and Denise.
- Special slot for adding an (optional) internal 1024x1024, 8 bit plane, color graphics, video DRAM based, graphics board. This memory will be fully addressable by the Agnes Blitter.
- Built-in Hard Disk Controller (SCSI).

- 1.76MB (formatted) Floppy Disk Drive.
- If possible, higher quality sound output.
- 1MB of "chip" (video) RAM, 1MB of "fast" RAM. Sockets for additional 2MB of "FAST" RAM on motherboard.
- Expansion slots fully compatible with A2000. Additional 32-bit expansion slot (for adding 32-bit wide "fast" RAM, etc.).
- All other I/O ports as A2000.
- Ability to run both AmigaDOS and Unix.
- First Prototype February 1988.
- Production startup, July 1988.

2.16. Super B52 (A500 case, 68020 CPU).

This is basically a 68020 based machine in an A500 case. Currently plans are not to include MMU and cache chip although this is open to debate. Cost is main consideration here. Specifications are:

- 68020 running at 15MHz.
- 1MB of "chip" memory, Highres Fat Agnes and Denise.
- Built-in SCSI connector for external Hard Disk Drive (leaves expansion bus open even if hard disk is being used).
- Built-in Battery Backed up real time clock.
- Optional 2MB, 32-bit wide, Ram Expansion cartridge with 68881 floating point processor. This plugs into same position as current A500 512K RAM Expansion module.
- Possibly a 1.76MB (formatted) Floppy Disk Drive, if cost target can be met and PAULA chip can be jacked up to double the transfer rate with downward compatibility.
- Expansion BUS and other I/O ports same as A500.
- First Prototype end January 1988. Production June 1988.
- Cost target $400 to $450. (Suggested List Price $1195 to $1395).
- Cost target of 2MB Ram expansion module with FPC, $250.

2.17. NYIT Genlock and Framegrabber.

Working with NYIT (CGL). Draft contract ready and waiting to be signed off. Current schedule is for earliest production startup in January 1988.

3. PC Project Descriptions.

Below is a short description of the PC Projects.

3.1. PC-1.

BSW Project. Looks good so far.

- PCB production starts in CETL on Aug 17.
- Final Assembly start in BSW on September 28.
- Cost (512KB) should be around $260, excluding MS-DOS Royalty. MS-DOS Royalty is $10 (assumes minimum MS-DOS shipments of 40K per quarter, else $15).

3.2. PC10-CR (XT).

PC10/20 replacement. Tooling orders will be released next week. Need another rev of PCB. Features of this machine are:

- 10MHZ, 8088 CPU. Three selectable clock speeds: 4.77, 7.16 and 9.54 MHz.
- 640KB Ram. Battery backed up RTC, 75W power supply.
- 101/102 Key Keyboard.
- Parallel, serial and mouse ports on motherboard.
- Mono and color graphics and 132 column modes built-in on motherboard
- Special connector for "XT" interface Hard Disk Drive. When used, hard disk drive controller does not use an expansion slot.
- 3 free expansion slots, even when 20MB HDD installed.
- 1 x 360KB Floppy Drive with space for second 5.25" peripheral as well as an internal 3.5" Hard Disk Drive.
- Planned Production Startup Date in Far East, October 15.
- Landed cost WC, $315, excluding MS-DOS Royalty of $10-$15.

3.3. PC40-CR (AT).

Same case as PC10-CR with different front bezel. Schedule is:

- 12MHz, 80286 CPU. Switchable clock speeds of 8, 10 and 12MHz.
- 1MB RAM, battery backed up clock, 112W power supply.
- 101/102 Key Keyboard. "Key lock" on front bezel.
- Parallel, serial and mouse ports on motherboard.
- MFM and RLL Hard Disk Controller (software selectable) built-in on motherboard.
- Hercules, CGA, EGA and extended EGA (640 x 480) graphics modes built-in. 132 columns display in both mono and color.
- 3 free expansion slots with hard disk installed.
- 1 x 1.2MB 5.25" Floppy Disk Drive with room for an additional 5.25" peripheral.
- 45MB, 28ms average access time, 3.5" internal hard disk standard.
- Production startup in Far East tergeted for December 7.
- Cost target (with 45MB hard disk) $990, landed WC.

3.4. PC80 (386 machine in current PC40 case).

BSW Project. This will be a "high-end" 386 machine. Initially we will OEM a 386 board from Far East and house in current PC40 case. This can get us to market very fast. Probably by December 1986. BSW can later do a in-house developed motherboard.

3.5. Baby 386 (XT/AT case).

This machine will use same case as the new PC10-CR and PC40-CR. Different front bezel only. Schedule and cost still to be finalised.

brought to you by
andy finkel